ON Semiconductor®

2- and 4-Channel Low Capacitance ESD Protection Arrays

CM1224

Features

- Two or four channels of ESD protection
- Provides ESD protection to IEC61000-4-2 Level 4
  - ±8kV contact discharge
- Low channel input capacitance of 0.7pF typical
- Minimal capacitance change with temperature and voltage
- Channel input capacitance matching of 0.02pF typical is ideal for differential signals
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Low clamping voltage (V_{CLAMP}) at 10V
- Low Dynamic resistance (R_{DYN}) at 1.08Ω
- Each I/O pin can withstand over 1000 ESD strikes*
- Available in SOT and MSOP lead-free packages

Applications

- USB 2.0 ports at 480Mbps in desktop PCs, notebooks and peripherals
- IEEE1394 Firewire® ports at 400Mbps / 800Mbps
- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- General purpose high-speed data line ESD protection

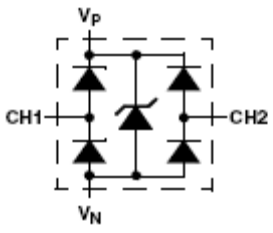
Product Description

The CM1224 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N, offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1224 protects against ESD pulses up to ±8kV per the IEC 61000-4-2 standard.

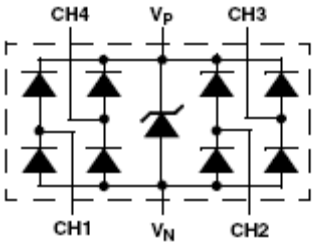
These devices are particularly well-suited for protecting systems using high-speed ports such as USB 2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, as well as DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required.

The CM1224 family of devices has lead-free finishing in a small package footprint.

Block Diagram



CM1224-02SR



CM1224-04SO
CM1224-04MR

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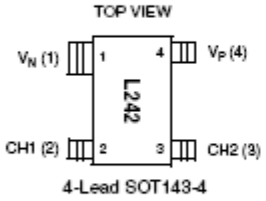
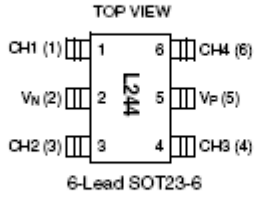
Publication Order Number:
CM1224/D

Package/Pinout Diagrams

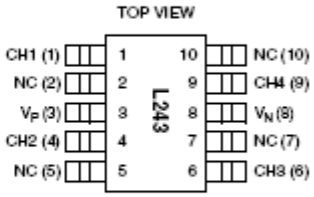
PACKAGE / PINOUT DIAGRAMS



4-Lead SOT143-4



6-Lead SOT23-6



10-Lead MSOP-10

Pin Configuration

2-CHANNEL, 4-LEAD SOT143-4 PACKAGE			
PIN	**NAME**	**TYPE**	**DESCRIPTION**
1	V_N	GND	Negative voltage supply rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V_P	PWR	Positive voltage supply rail

4-CHANNEL, 6-LEAD SOT23-6 PACKAGES			
PIN	**NAME**	**TYPE**	**DESCRIPTION**
1	CH1	I/O	ESD Channel
2	V_N	GND	Negative voltage supply rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V_P	PWR	Positive voltage supply rail
6	CH4	I/O	ESD Channel

4-CHANNEL, 10-LEAD MSOP-10 PACKAGES			
PIN	**NAME**	**TYPE**	**DESCRIPTION**
1	CH1	I/O	ESD Channel
2	NC		No Connect
3	V_P	PWR	Positive voltage supply rail
4	CH2	I/O	ESD Channel
5	NC		No Connect
6	CH3	I/O	ESD Channel
7	NC		No Connect
8	V_N	GND	Negative voltage supply rail
9	CH4	I/O	ESD Channel
10	NC		No Connect

Ordering Information

PART NUMBERING INFORMATION				
			Lead-free Finish	
# of Channels	Leads	Package	Ordering Part Number[1]	Part Marking
2	4	SOT143-4	CM1224-02SR	L242
4	6	SOT23-6	CM1224-04SO	L244
4	10	MSOP-10	CM1224-04MR	L243

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
Operating Supply Voltage (V_P - V_N)	6.0	V
Operating Temperature Range	–40 to +85	℃
Storage Temperature Range	–65 to +150	℃
DC Voltage at any channel input	(V_N - 0.5) to (V_P + 0.5)	V

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Operating Temperature Range	–40 to +85	℃
Package Power Rating SOT23-3, SOT143-4,SOT23-5 and SOT23-6 Packages MSOP-10 Package	 225 400	 mW mW

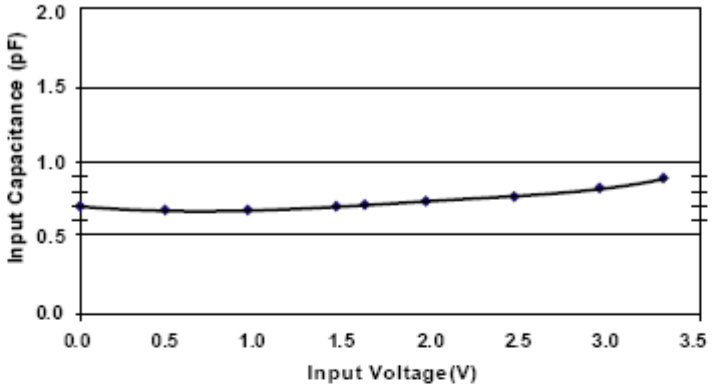
ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Operating Supply Voltage (V_P-V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P-V_N)=3.3V			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA; T_A=25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	 V V
I_{LEAK}	Channel Leakage Current	T_A=25°C; V_P=5V, V_N=0V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V	0.60	0.70	0.80	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V		0.02		pF
V_{ESD}	ESD Protection - Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard	Notes 2 and 3; T_A=25°C	±8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A=25°C, I_{PP} = 1A, t_P = 8/20μS; Note 3		 +10.0 –1.8		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1A, t_P = 8/20μS Any I/O pin to Ground; Note 3		 1.08 0.66		 Ω Ω

Note 1: All parameters specified at T_A = –40°C to +85°C unless otherwise noted.
Note 2: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 3.3V, V_N grounded.
Note 3: These measurements performed with no external capacitor on V_P (V_P floating).

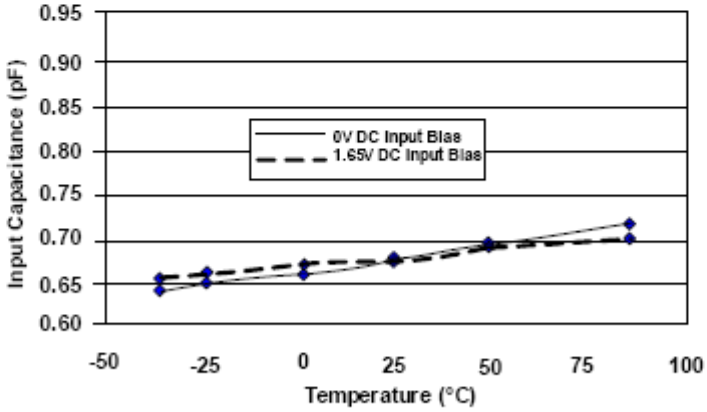
Performance Information

Input Channel Capacitance Performance Curves



Typical Variation of C_{IN} vs. V_{IN}

(f=1MHz, V_P = 3.3V, V_N = 0V, 10kΩ between V_P and 3.3V supply, 0.1 µF chip capacitor between V_P and V_N, 25°C)



Typical Variation of C_{IN} vs. Temp

(f=1MHz, V_{IN}=30mV, V_P = 3.3V, V_N = 0V,10kΩ between V_P and 3.3V supply, 0.1 µF chip capacitor between V_P and V_N)

Performance Information (cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

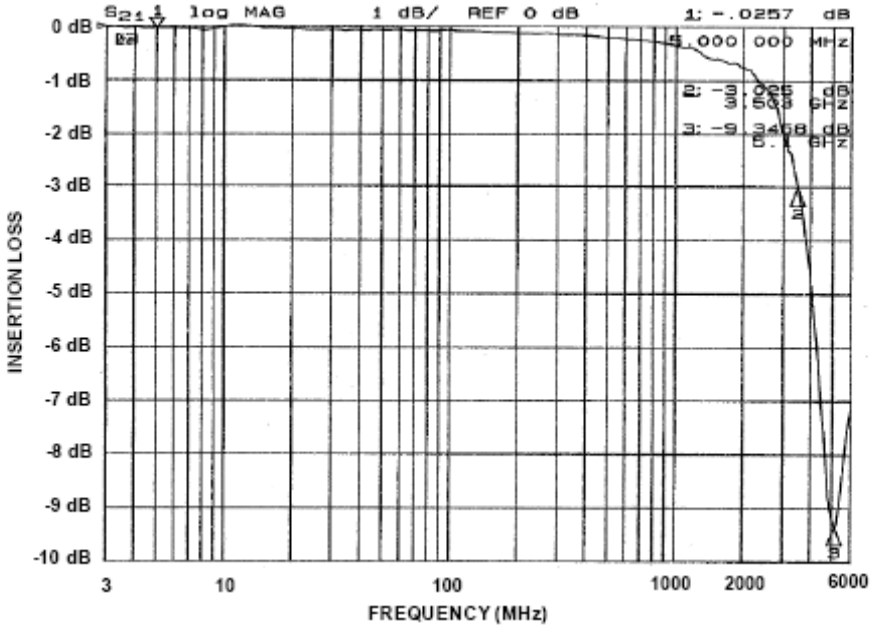


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias, V_P=3.3V)

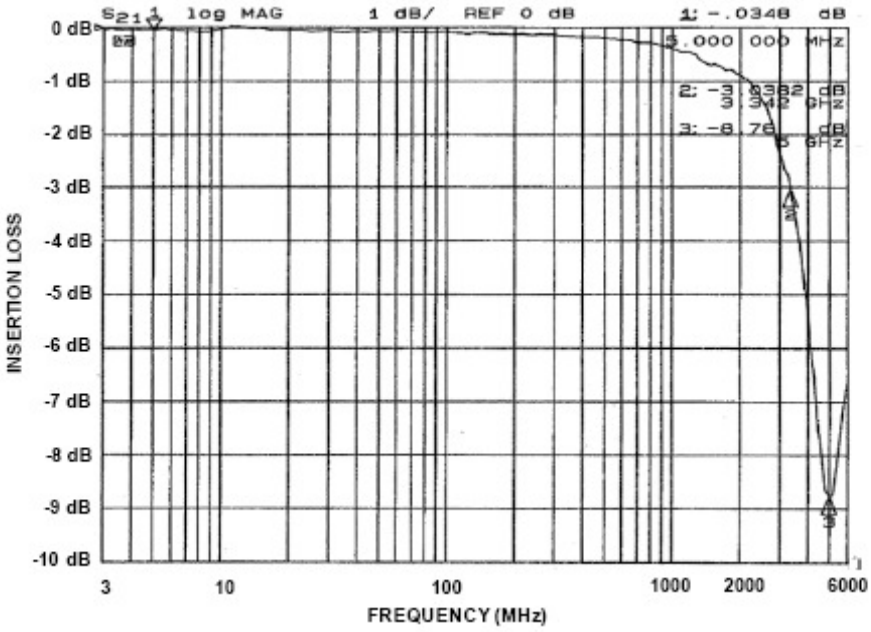


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias, V_P=3.3V)

Application Information

Design Considerations

To realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Application of Positive ESD Pulse between Input Channel and Ground illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from 0 to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1224 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22µF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned earlier should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Note AP209, “Design Considerations for ESD Protection,” in the Applications section at www.calmicro.com.

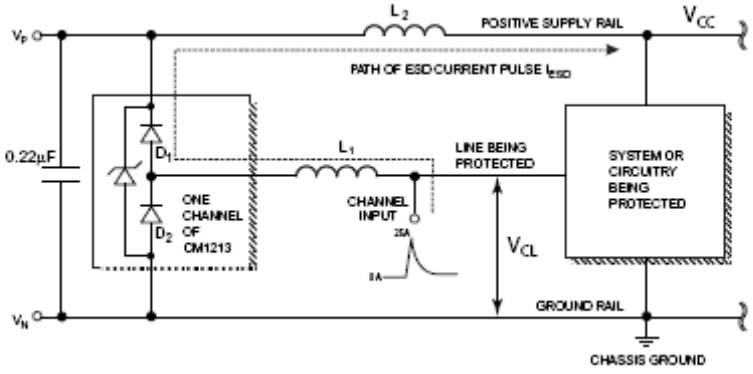


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

Mechanical Details

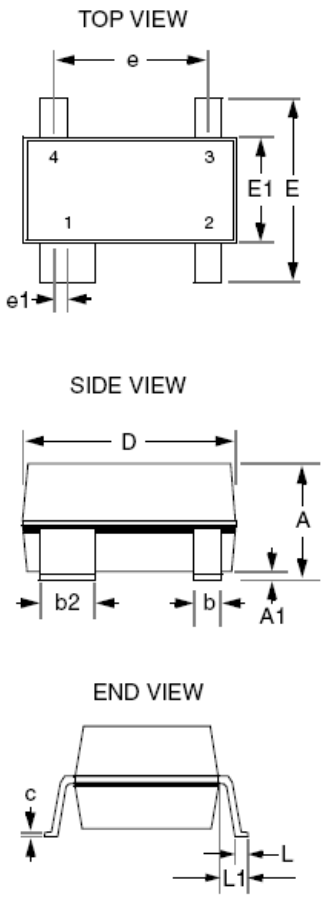
The CM1224 is available in SOT143-4, SOT23-6, and MSOP-10 packages with a lad-free finishing option. The various package drawings are presented below.

SOT143-4 Mechanical Specifications

Dimensions for CM1224-02SR devices supplied in 4-pin SOT143 packages are presented below.

PACKAGE DIMENSIONS				
Package	SOT143			
Pins	4			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.80	1.22	0.031	0.048
A1	0.05	0.15	0.002	0.006
b	0.30	0.50	0.012	0.019
b2	0.76	0.89	0.030	0.035
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.119
E	2.10	2.64	0.082	0.103
E1	1.20	1.40	0.047	0.055
e	1.92 BSC		0.075 BSC	
e1	0.20 BSC		0.008 BSC	
L	0.4	0.6	0.016	0.024
L1	0.54 REF		0.021 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

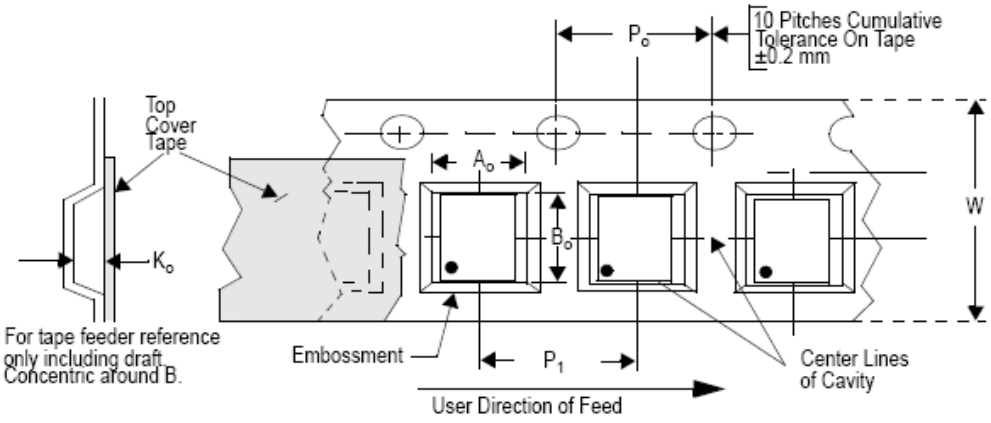
Mechanical Package Diagrams



Package Dimensions for SOT143

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1224-02SR	2.92 X 2.37 X 1.01	2.60 X 3.15 X 1.20	8mm	178mm (7")	3000	4mm	4mm



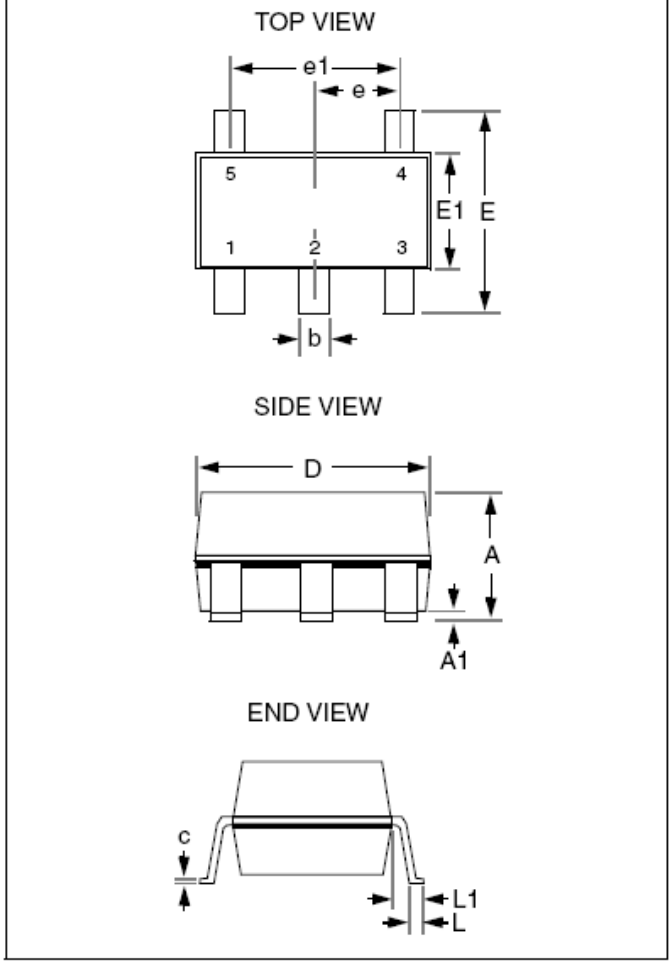
Mechanical Details (cont'd)

SOT23-6 Mechanical Specifications

CM1224-04SO devices are packaged in 6-pin SOT23 packages. Dimensions are presented below.

PACKAGE DIMENSIONS				
Package	SOT23-6 (JEDEC name is MO-178)			
Pins	6			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

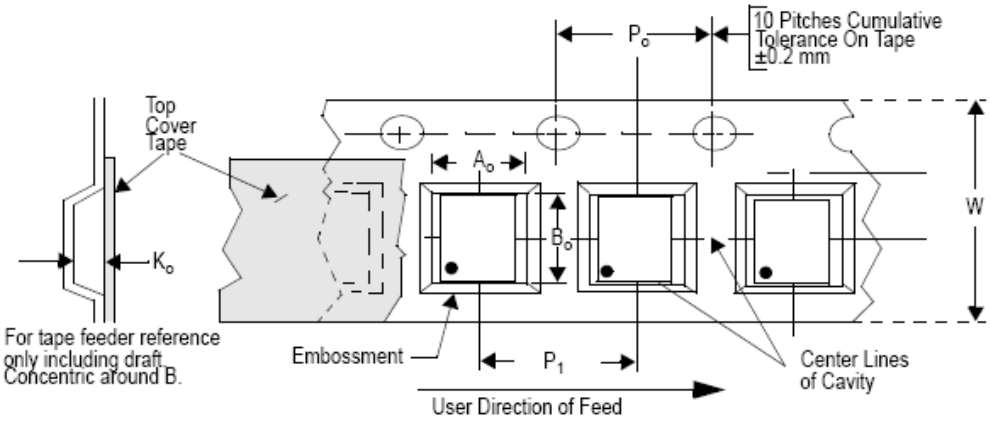
Mechanical Package Diagrams



Package Dimensions for SOT23-6

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1224-04SO	2.90 X 2.80 X 1.45	3.20 X 3.20 X 1.40	8mm	178mm (7")	3000	4mm	4mm

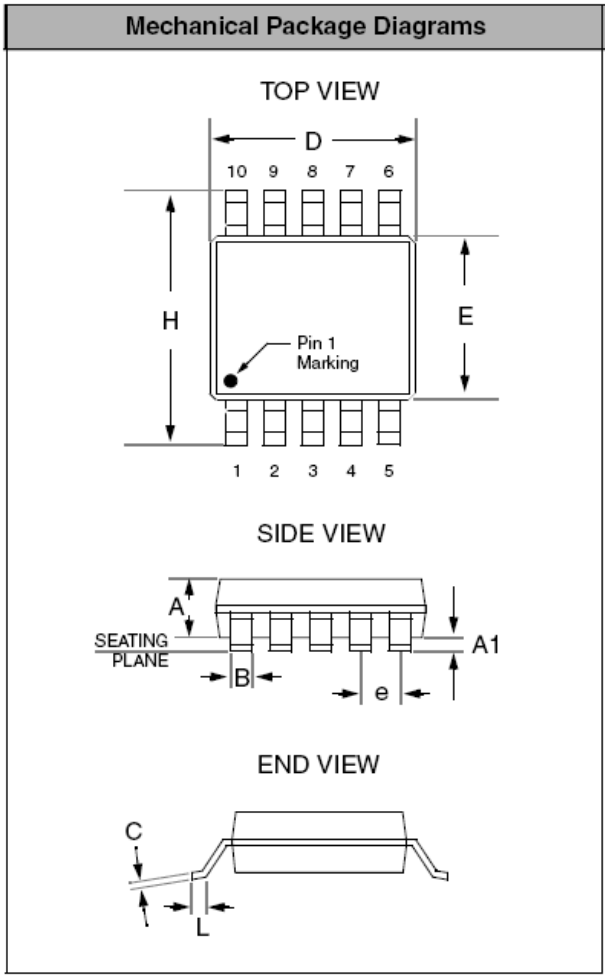


Mechanical Details (cont'd)

MSOP-10 Mechanical Specifications, 10 pin

The CM1224-04MR 10-lead MSOP package dimensions are presented below.

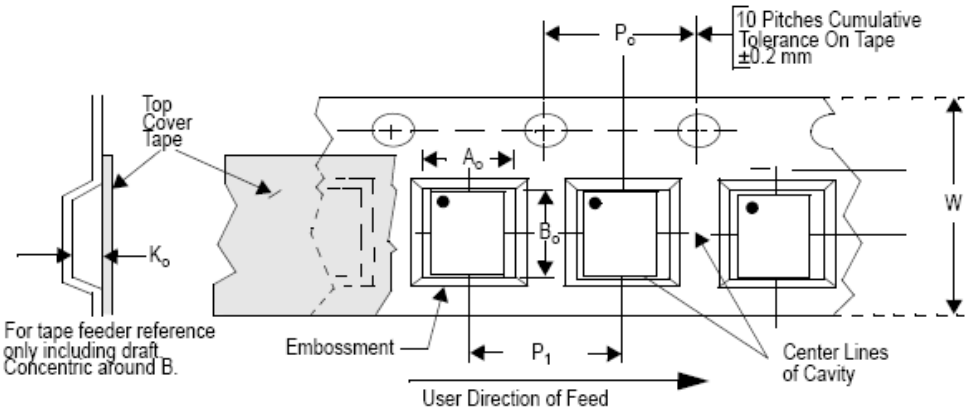
PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.17	0.27	0.007	0.013
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.0137	0.029
# per tape and reel	4000			
Controlling dimension: millimeters				



Package Dimensions for MSOP-10

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1224-04MR	3.00 X 3.00 X 0.85	3.30 X 5.30 X 1.30	12mm	330mm (13")	4000	4mm	8mm



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